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1.(Currently Amended) A monolithic integrated circuit for multiplying together a digitized multiplier signal value and a digitized multiplicand signal value, said monolithic integrated circuit comprising:

an input interface that receives said multiplicand and provides a received multiplicand indicative thereof;

a first bi-directional shifting device that includes a first logical assignment circuit to shift data bits of said received multiplicand in response to a first shift command signal, and provides a first shifted signal indicative thereof;

a second bi-directional shifting device that includes a second logical assignment circuit to shift data bits of said received multiplicand in response to a second shift command signal, and provides a second shifted signal indicative thereof;

means for summing said first and second shifted signals to provide a summed signal value that is indicative of the product of said multiplier signal value and said multiplicand signal value; and

a control device that receives a signal indicative of said multiplier, and generates said first and second shift command signals indicative of said multiplier signal value.

2.(Previously Presented) The monolithic integrated circuit of claim 1, comprising a memory device for storing said summed signal, and for providing past values of said summed signal value.

3.(Previously Presented) The monolithic integrated circuit of claim 2, wherein said means for summing receives and sums a signal value from said memory device indicative of a past value of said summed signal value with said first and second shifted signals to provide said summed signal value.

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4.(Previously Presented) The monolithic integrated circuit of claim 1, wherein said first bi-directional shifting device comprises a first sign inverter that receives and inverts the sign of said received multiplicand to provide a sign inverted received multiplicand signal that is input to said first logical assignment circuit for bit shifting.

5.(Previously Presented) The monolithic integrated circuit of claim 4, wherein said second bi-directional shifting device comprises a second sign inverter that receives and selectively inverts the sign of said received multiplicand to provide a second sign inverted received multiplicand signal that is input to said second logical assignment circuit for bit shifting.

6.(Previously Presented) The monolithic integrated circuit of claim 1, wherein said control unit generates a first sign inversion command signal in response to said multiplier value, wherein said first sign inversion signal is input to said first sign inverter to selectively enable the sign inversion.

7.(Previously Presented) A monolithic integrated circuit on a monolithic integrated circuit for multiplying together a digitized multiplier signal value and a digitized multiplicand signal value, comprising:

an input interface that receives said multiplicand and provides a received multiplicand indicative thereof;

first means for bi-directionally shifting data bits of said received multiplicand in response to a first shift command signal, and for providing a first shifted signal indicative thereof;

second means for bi-directionally shifting data bits of said received multiplicand in response

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to a second shift command signal, and for providing a second shifted signal indicative thereof;

means for summing said first and second shifted signals to provide a summed signal value that is indicative of the product of said multiplier and said multiplicand; and

a control device that receives a signal indicative of said multiplier that is a binary coded number using canonical form, and generates said first and second shift command signals indicative of said multiplier value.

8.(Previously Presented) The monolithic integrated circuit of claim 7, comprising a memory device for storing said summed signal, and for providing past values of said summed signal value.

9.(Previously Presented) The monolithic integrated circuit of claim 8, wherein said means for summing receives and sums a signal value from said memory device indicative of a past value of said summed signal value with said first and second shifted signals to provide said summed signal value.

10.(Previously Presented) The monolithic integrated circuit of claim 7, wherein said first means for bi-directionally shifting comprises a first sign inverter that receives and inverts the sign of said received multiplicand to provide a sign inverted received multiplicand signal that is input to said first logical assignment circuit for bit shifting.

11.(Previously Presented) The monolithic integrated circuit of claim 10, wherein said second means for bi-directionally shifting comprises a second sign inverter that receives and selectively inverts the sign of said received multiplicand to provide a second sign inverted received multiplicand

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signal that is input to said second logical assignment circuit for bit shifting.

12.(Canceled)

13.(Canceled)

14.(Canceled)

15.(Canceled)

16.(Canceled)

17.(Canceled)

18.(Canceled)

19.(New) A monolithic integrated circuit for multiplying together a digitized multiplier signal value and a digitized multiplicand signal value, said monolithic integrated circuit comprising:

a first bi-directional shifting device that includes a first logical assignment circuit to shift data bits of said digitized multiplicand signal value in response to a first shift command signal, and provides a first shifted signal indicative thereof;

a second bi-directional shifting device that includes a second logical assignment circuit to shift data bits of said digitized multiplicand signal value in response to a second shift command

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signal, and provides a second shifted signal indicative thereof;

a summer that sums said first and second shifted signals to provide a summed signal value; and

a control device that receives a signal indicative of said multiplier signal value, and generates said first and second shift command signals indicative of said multiplier signal value.

20.(New) The monolithic integrated circuit of claim 19, comprising a memory device for storing said summed signal, and for providing past values of said summed signal value.

21.(New) The monolithic integrated circuit of claim 20, wherein said summer receives and sums a signal value from said memory device indicative of a past value of said summed signal value with said first and second shifted signals to provide said summed signal value.

22.(New) The monolithic integrated circuit of claim 19, wherein said first bi-directional shifting device comprises a first sign inverter that receives and inverts the sign of said digitized multiplicand signal value to provide a sign inverted received multiplicand signal that is input to said first logical assignment circuit for bit shifting.

23.(New) The monolithic integrated circuit of claim 22, wherein said second bi-directional shifting device comprises a second sign inverter that receives and selectively inverts the sign of said digitized multiplicand signal value to provide a second sign inverted received multiplicand signal that is input to said second logical assignment circuit for bit shifting.

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24.(New) The monolithic integrated circuit of claim 19, wherein said control unit generates a first sign inversion command signal in response to said multiplier signal value, wherein said first sign inversion signal is input to said first sign inverter to selectively enable the sign inversion.

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